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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,873	KUBLER ET AL.	
	Examiner	Art Unit	
	VENKATESH HALIYUR	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/16/2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-60 (1-21 are canceled)* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/17/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on 06/16/2008 has been considered and is insufficient to overcome the references. However a new ground(s) of rejection has been made using a newly found Chan et al reference. Therefore the rejection of claims communicated via previous office action has been withdrawn. Rejection follows.

2. Claims 22-60 is pending in the application. Claims 1-21 are cancelled.

Claim Rejections – 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 22-24, 29-32, 33-37, 42-45, 46, 49-50, 54-57, and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henley et al (U.S Patent No. 5,526,353) in view of Chan et al [US Pat: 5,550,861].

Regarding claim 22, Henley et al teach a voice communication circuit comprising:

- at least one processor (FIG. 2, 210, 220) capable of packetizing digitized voice information to produce at least one voice packet (column 5, lines 5-8); Henley et al further disclose the packet assembly circuit is microprocessor based integrated circuit in column 7, lines 46-54);
- a buffer (FIG. 2, 250) capable of storing the at least one voice packet (column 10, lines 40-45);
- interface circuitry (FIG. 2) capable of communicatively coupling the buffer with one of a plurality of interchangeable network interfaces (FIG. 1,130, 170, column 5, lines 14-16), each of the plurality of interchangeable network interfaces supporting communication of voice packets via an associated type of communication network (FIG. 1,150, column 9, lines 13-17);
- the at least one processor (FIG. 2, 210) capable of determining the associate type of communication network supported by the one of the plurality of interchangeable network interfaces in communication with the interface circuitry (column 7, lines 37-42; Henley et al teach the microprocessor-driven packet assembly and disassembly circuits are equipped in separate computers. Thus making communication between the plurality of nodes possible through the interchangeable interfaces claimed previously. Additionally, it is further disclosed that the present invention provides a

system for communicating audio data in the packet-based computer network - column 8, lines 65-66. Therefore the associate type of communication network must be supported by the interfaces);

- the at least one processor (FIG. 2, 210) capable of arranging the transmission of voice packets via the one of the plurality of interchangeable network interfaces based upon the associated type of communication network (column 7, 19-26). Henley et al disclosed that the packet assembly circuit performs conversion of audio data into digital packet data for transmission over the network but fails to disclose that transmission of voice packets is performed via the plurality of interchangeable network interfaces. However, Chan et al disclosed a method of providing plurality of modularly configurable or interchangeable interfaces for the peripheral components of a host device using PCMCIA interface circuitry to transmit packets to an associated network (item 30 of Fig 2, col 2, lines 40-67, col 3, lines 1-43). Therefore it would have been obvious for one of the ordinary skill in the art at the time the invention was made to use the method of providing plurality of modularly configurable or interchangeable interfaces for a host device to transmit voice packets to a network as taught by Chan et al in the system of Henley et al to perform the function of transmitting voice packets over plurality of interchangeable interfaces by the host processor based on the type of communication network. One is motivated as such in order to provide a modular interface circuitry to transmit packets over plurality interchangeable interfaces to a network.

Regarding claims 23 and 37, Henley et al teach the voice communication circuit of claim 22 wherein the voice packets are packetized according to an Internet protocol (IP) (column 4, lines 6-7).

Regarding claim 24, Henley et al disclose the voice communication circuit of claim 23 wherein the Internet protocol (IP) comprises the transmission control protocol (TCP)/Internet protocol (IP) (column 4, lines 6-7).

Regarding claims 29, 42, and 54, Henley et al teach the voice communication circuit of claims 22, 36, and 50, respectively, wherein the associated type of communication network comprises a wired network (FIG. 1).

Regarding claims 30, 43, and 55, Henley et al teach the voice communication circuit of claims 29, 42, and 50, respectively, wherein the wired network comprises an Ethernet compatible network (FIG. 1,140).

Regarding claims 31,44, and 56, Henley et al teach the voice communication circuit of claims 29, 42, and 50, respectively, wherein the wired network comprises a conventional telephone switching network (FIG. 1, 110, 160, column 8, lines 55-63).

Regarding claim 33, Henley et al teach the voice communication circuit of claim 22 further comprising: the at least one processor capable of reducing the quantity of voice packets communicated via a communication network by changing the packetization based upon a level of voice activity (column 5, lines 65-67, column 6, lines 1-5).

Regarding claim 34, Henley et al teach the voice communication circuit of claim 22 further comprising converter circuitry capable of converting a voice stream into digitized voice information (column 7, lines 19-21).

Regarding claims 35 and 49, Henley et al teach the voice communication circuit of claims 22 and 46, wherein the voice stream comprises an analog signal (column 7, lines 19-21).

Regarding claim 36, Henley et al teach a voice communication circuit comprising:

- interface circuitry (FIG. 2) capable of communicatively coupling with one of a plurality of interchangeable network interfaces (FIG. 1,130, 170, column 5, lines 14-16), each of the plurality of interchangeable network interfaces capable of communicating via an associated type of communication network to receive at least one voice packet (FIG. 1,150, column 9, lines 13-20);
- a buffer (FIG. 2, 250) capable of storing the at least one voice packet (column 10, lines 40-45);
- at least one processor (FIG. 2, 210) capable of depacketizing the at least one voice packet to produce digitized voice information (FIG. 7, column 16, I lines 17-22);
- the at least one processor (FIG. 2, 210) capable of determining the associate type of communication network supported by the one of the plurality of interchangeable network interfaces in communication with the interface circuitry (column 7, lines 37-42; Henley et al teach the microprocessor-driven packet assembly and disassembly circuits are equipped in separate computers. Thus making communication

between the plurality of nodes possible through the interchangeable interfaces claimed previously. Additionally, it is further disclosed that the present invention provides a system for communicating audio data in the packet-based computer network - column 8, lines 65-66. Therefore the associate type of communication network must be supported by the interfaces); and

- the at least one processor (FIG. 2, 210) capable of arranging the reception of the at least one packet via the one of the plurality of interchangeable network interfaces based upon the associated type of communication network (column 7, 19-26). Henley et al disclosed that the packet assembly circuit performs conversion of audio data into digital packet data for transmission over the network but fails to disclose that transmission of voice packets is performed via the plurality of interchangeable network interfaces. However, Chan et al disclosed a method of providing plurality of modularly configurable or interchangeable interfaces for the peripheral components of a host device using PCMCIA interface circuitry to receive packets from an associated network (item 30 of Fig 2, col 2, lines 40-67, col 3, lines 1-43). Therefore it would have been obvious for one of the ordinary skill in the art at the time the invention was made to use the method of providing plurality of modularly configurable or interchangeable interfaces for a host device to receive voice packets from a network as taught by Chan et al in the system of Henley et al to perform the function of receiving voice packets over plurality of interchangeable interfaces by the host processor based on the type of communication network. One is motivated as such in order to provide a modular

interface circuitry to receive packets over plurality interchangeable interfaces to a network.

Regarding claim 46, Henley et al teach t he voice communication circuit of claim 36 further comprising: converter circuitry capable of converting the digitized voice information to produce a voice stream (column 7, lines 27-31).

Regarding claim 50, Henley et al teach a machine-readable storage having stored thereon a computer program having a plurality of code sections for implementing a voice communication system, the voice communication system capable of accepting at any point in time one of a plurality of interchangeable network interfaces, each of the interchangeable network interfaces for use with an associated type of communication network, the code sections executable by a machine for causing the machine to perform the operations comprising:

- detecting the presence of an interchangeable network interface (column 3, lines 32-34);

- determining the associated type of communication network for use with the detected interchangeable network interface (column 7, lines 37-42; Henley et al teach the microprocessor-driven packet assembly and disassembly circuits are equipped in separate computers. Thus making communication between the plurality of nodes possible through the interchangeable interfaces claimed previously. Additionally, it is further disclosed that the present invention provides a system for communicating audio data in the packet-based computer network - column 8, lines 65-66. Therefore the associate type of communication network

must be supported by the interfaces);

- establishing a packet voice call via the associated type of communication network (column 4, lines 18-24);

- converting analog voice information to transmit voice packets (column 5, lines 5-8, lines 22-30);

- sending the transmit voice packets via the associated type of communication network using the interchangeable network interface (column 1, lines 4-10);

- receiving voice packets via the associated type of communication network using the interchangeable network interface (column 1, lines 4-10); and

- converting the received voice packets to analog voice information (column 7, lines 27-31). Henley et al disclosed that the packet assembly circuit performs conversion of audio data into digital packet data for transmission over the network but fails to disclose that transmitting or receiving voice packets is performed via the plurality of interchangeable network interfaces. However, Chan et al disclosed a method of providing plurality of modularly configurable or interchangeable interfaces for the peripheral components of a host device using PCMCIA interface circuitry to either receive or transmit packets to an associated network (item 30 of Fig 2, col 2, lines 40-67, col 3, lines 1-43). Therefore it would have been obvious for one of the ordinary skill in the art at the time the invention was made to use the method of providing plurality of modularly configurable or interchangeable interfaces for a host device to either receive from or transmit

voice packets to a network as taught by Chan et al in the system of Henley et al to perform the function of either receiving or transmitting voice packets over plurality of interchangeable interfaces by the host processor based on the associated type of communication network. One is motivated as such in order to provide a modular interface circuitry to either receive or transmit packets over plurality interchangeable interfaces to a network.

Regarding claim 57, Henley et al teach the machine-readable storage of claim 50 wherein converting analog voice information to transmit voice packets comprises: reducing the volume of transmit voice packets based upon a level of voice activity (column 5, lines 65-67, column 6, lines 1-5).

Regarding claim 60, Henley et al teach the machine readable storage of claim 50 further comprising: adapting call setup of the voice communication system based upon the type of communication network (column 11, lines 65-68, column 12, lines 1-5).

Regarding claims 32 and 45, Henley et al teach the voice communication circuit of claims 22 and 36. However, Henley et al fail to explicitly teach the interface circuitry is compatible with a Personal Computer Memory Card Interface Association (PCMCIA) standard. Chan et al disclosed a system and method for interfacing voice communication circuit compatible with PCMCIA standard. According to the teaching, the digital entertainment terminal 12 of Fig 1 comprising personal computer memory card interface adapter (PCMCIA) port 14 of Fig 1 (column 3, lines 44-67,col 4, lines 1-14). Therefore, it would have been

obvious to one with ordinary skill in the art at the time of the invention was made to use the interface circuitry compatible with a PCMCIA standard as taught by Chan et al in the system of Henley et al for the interface circuitry to be compatible with a Personal Computer Memory Card Interface Association (PCMCIA) standard. One is motivated as such to allow a two way communication between the system and the flash memory module, or smart card. When such module is connected to the interface, it utilizes data processing capabilities such as buffering and facilitating modem communication.

5. Claims 25-26, 38-39, 51-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henley et al. (U.S Patent No: 5,526,353) and Chan et al [US Pat: 5,550,861] further in view of Heath et al (U.S Patent No. 5,231,646).

Regarding claims 25, 38, and 51, Henley et al teach the voice communication circuit of claims 22, 36, and 50, respectively. Henley et al and Chan et al fail to explicitly teach the associated type of communication network is a wireless packet network. Heath et al teach a radio communication system capable of being employed in a small geographic area such as a long distance communication system. It is disclosed that an object of the invention is to provide a local area network using a predetermined protocol to connect nodes with wireless radio frequency (RF) links instead of hard wired links (column 2, lines 45-48). Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention was made to modify the teachings of Henley et al and

Chan et al to make the associate type of communication network a wireless packet network as taught by Heath et al. One is motivated as such to enable computers to share resources and communicate with computers in other networks over a long distance communication system (column 2, lines 19-26).

Regarding claim 26, 39, and 52, Henley et al teach the voice communication circuit of claims 25, 38, and 51, respectively. Henley et al and Chan et al fail to explicitly teach the wireless packet network communicates at approximately 2.4 gigahertz. Heath et al disclose the present invention can employ a preferred band 2400 MHz or 2.4 GHz for radio communication (column 6, lines 35-41). Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention was made to modify the teachings of Henley et al to enable the wireless packet network communicating at approximately 2.4 gigahertz as taught by Heath et al. One is motivated as such to achieve greater signal penetration through office walls and to reduce interference between neighboring networks, and to resolve the problem of multipath interference (column 6, lines 50-67).

6. Claims 27-28, 40-41, 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henley et al. (U.S Patent No: 5,526,353) and Heath et al (U.S Patent No. 5,231,646) and Chan et al [US Pat: 5,550,861] further in view of Avery et al (US Pat: 5,287,384).

Regarding claims 27, 40 53, Henley et al teach the voice communication circuit but fail to teach the wireless packet network communication (column 5, lines 5-8). Heath et al disclosed that the interface wireless packet network that communicates at 2.4 GHz (column 6, lines 35-41). Chan et al disclosed a wireless data communication network circuitry (item 36 and 38 of Fig 2) for performing the pager functions via the PCMCIA card (col 2, lines 58-62, Figs 1-2). However Henley et al, Heath et al and Chan et al fail to teach the wireless packet network communicates using a frequency hopping spread spectrum technique. Avery et al teach a wireless data communication network employing frequency hopping spread spectrum transmission technique (abstract). Hence it would have been obvious to one with ordinary skill in the art at the time of the invention was made to modify the teachings of Henley et al, Heath et al and Chan et al to allow the wireless packet network communicate using a frequency hopping spectrum technique as taught by Avery et al. One is motivated as such to build a robust network that is resistant to interferences from other adjacent radio frequency networks (column 2, lines 49-58).

Regarding claims 28, 41, Henley et al teach the voice communication circuit, but fail to teach the wireless packet network communication (column 5, lines 5-8). Heath et al disclosed that the interface wireless packet network that communicates at 2.4 GHz (column 6, lines 35-41) and Chan et al disclosed a wireless data communication network circuitry (item 36 and 38 of Fig 2) for performing the pager functions via the PCMCIA card (col 2, lines 58-62, Figs 1-2). However Henley et al, Heath et al and Chan et al fail to teach the wireless packet network communicates using a direct sequence

spread spectrum technique. Avery et al disclose the direct sequence spread spectrum (DSSS) technique was implemented by manufacturers when spread spectrum technology was first allowed by the Federal Communications Commission (column 2, lines 59-62). Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention was made to modify the teachings of Henley et al, Heath et al and Chan et al to allow the wireless packet network communicate using a direct sequence spectrum technique as taught by Avery et al. One is motivated as such in order to reduce the cost of the communication system while retaining the ability to retrofit certain aspects of the existing designs (column 3, lines 12-14).

7. Claims 47, 48, 58, and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henley et al. (U.S Patent No: 5,526,353) and Chan et al [US Pat: 5,550,861] further in view of Sharman et al (U.S Patent No. 5,774,854).

Regarding claims 47 and 48, Henley et al teach the voice communication circuit of claim 46. However, Henley et al and Chan et al fail to explicitly teach the at least one processor capable of adjusting the buffering of voice packets in order to minimize gaps in the voice stream and the adjusting is based upon a propagation delay of a communication network. Sharman teaches a text to speech system operating in real using an acoustic processor and a linguistic processor. Due to the computational time the linguistic processor requires to process data, future requests from the acoustic processor cannot be made. Thus gaps in the speech output often occur when the acoustic processor requests data from the linguistic processor. Sharman proposes a

solution to overcome the gaps in data by adjusting the buffer for minimal of output data so that future requests can be supplied in a timely manner (column 7, lines 39-48). Hence the propagation delay caused by the linguistic processor is a factor affecting the adjustment in the buffer for desired optimal output. Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention was made to modify the teachings of Henley et al and Chan et al to enable the processor to adjust the buffering of voice packets based on the propagation delay in order to minimize gaps in the voice stream as taught by Sharman. One is motivated as such to accurately halt the system based on the output in the event that an interruption occurs (abstract, column 2, lines 34-39).

Regarding claims 58 and 59, Henley et al teach the machine-readable storage of claim 50. However, Henley et al and Chan et al fail to explicitly teach converting the received voice packets to analog voice information comprises: buffering voice packets for an adjustable period of time to avoid gaps in the analog voice information. Sharman teaches a text to speech system operating in real using an acoustic processor and a linguistic processor. Due to the computational time the linguistic processor requires to process data, future requests from the acoustic processor cannot be made. Thus gaps in the speech output often occur when the acoustic processor requests data from the linguistic processor. Sharman proposes a solution to avoid the gaps in data by adjusting the buffer for minimal of output data so that future requests can be supplied in a timely manner (column 7, lines 39-48). Hence the propagation delay caused by the linguistic processor is a factor affecting the adjustment in the buffer for desired optimal output.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention was made to modify the teachings of Henley et al and Chan et al to enable the buffering of voice packets for an adjustable period of time based on the propagation delay to avoid gaps in the analog voice information as taught by Sharman. One is motivated as such to accurately halt the system based on the output in the event that an interruption occurs (abstract, column 2, lines 34-39).

Response to Arguments

8. Applicant's argument filed on 07/17/2008 with respect to claims 22-60 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Any inquiry concerning this communication or earlier communications should be directed to the attention to Venkatesh Haliyur whose phone number is 571-272-8616. The examiner can normally be reached on Monday-Friday from 9:00AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached @ (571)-272-7884. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (571)-272-2600 or fax to 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197(toll-free).

/Venkatesh Haliyur/

Examiner, Art Unit 2419

/Edan Orgad/

Supervisory Patent Examiner, Art Unit 2419